REMARKS

Claim 5 is amended, claims 7, 11, 13, 16-17, 24-30, 37, and 47-74 were previously canceled, and no claims are added; as a result, claims 1-6, 8-10, 12, 14-15, 18-23, 31-36, 38-46, and 75-94 are now pending in this application, and wherein claims 15, 18-23, 31-36, 38-46, and 75-93 are withdrawn.

No new matter has been added through the amendments to claim 5. Claim 5 has merely been amended to rewrite claim 5 in independent form to include all of the subject matter from the base claim and any intervening claims from which claim 5 previously depended.

Information Disclosure Statement

Applicant submitted an Supplemental Information Disclosure Statement and a 1449 Form on April 24, 2006. Applicant notes that an incorrect document was sent with the Supplemental Information Disclosure Statement of April 24, 2006. Applicant submits herewith another Supplemental Information Disclosure Statement and 1449 Form including the correct document, in addition to new documents, as submitted on the 1449 included with this response. Applicants respectfully requests that initialed copies of the 1449 Form be returned to Applicant's Representatives to indicate that the cited documents have been considered by the Examiner.

§102 Rejection of the Claims

Claims 1, 6, 8-10, 12, 14, and 94 were rejected under 35 U.S.C. § 102(a) for anticipation by Jerominek (U.S. 5,962,909). Applicant disagrees that Jerominek is a § 102(a) prior art reference. Applicant believes that the Jerominek patent is characterized as a reference under 35 U.S.C. § 102(e), and thus believes that Applicant also has the right as provided under 37 C.F.R. 1.131 to swear behind Jerominek. Therefore, Applicant does not admit that Jerominek is prior art and reserves the right, as provided for under 37 C.F.R. 1.131, to "swear behind" Jerominek at a later time. However, Applicant does not believe it is necessary to swear behind Jerominek at this time because claims 1, 6, 8-10, 12, 14, and 94 are not anticipated by Jerominek for at least the reasons stated below. Applicant respectfully traverses the 35 U.S.C. § 102 rejection of claims 1, 6, 8-10, 12, 14, and 94.

Claims 1, 6, 8-10, 12, 14, and 94 are not anticipated by Jerominek because Jerominek fails to disclose all of the subject matter included in each of claims 1, 6, 8-10, 12, 14, and 94 as arranged in the claims.[1] For example, claim 1 recites,

> a conductive structure embedded in a material layer having a plurality of vaporization temperatures, the material layer is formed on the electronic chip and the conductive structure includes a horizontal conductive interconnect and at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic chip,
>
> wherein the horizontal conductive interconnect is formed in and above a fill material.

Thus, claim 1 includes a horizontal conductive interconnect is formed in and above a fill material. The Office Action fails to point out in Jerominek a disclosure of a horizontal conductive interconnect, and merely states on page 5 of the Office Action, "wherein the horizontal conductive interconnect is formed in and above a fill material 6" Further, the Office Action on page 2 states, "a conductive structure 15 embedded in a material layer 4, 6, 10 having a plurality of vaporization temperatures," but fail to include an indication of where Jerominek discloses "a conductive structure *including a horizontal conductive interconnect and* at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic chip, wherein *the horizontal conductive interconnect is formed in and above a fill material*," as required by claim 1.

In contrast, Jerominek states,

> The microstructure 22 further comprises upper and lower dielectric layers 6 and 10. The upper dielectric layer 10 lies over the sensing layer 8 shown in FIG. 2F, and the lower dielectric layer 6 lies under the sensing layer 8 shown in FIG. 2F. The lower layer

[1] Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W. L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

> 6, in combination with the upper layer 10, embeds the sensing layer 8 shown on the FIG. 2F.[2]

However, there in no disclosure in Jerominek of "wherein the horizontal conducive interconnect is formed in and above a fill material," as included in claim 1. In addition, the Office Action fails to show how Jerominek discloses for example, "a material layer having a plurality of vaporization temperatures," as included in claim 1. The Office Action, for example on page 2, relies on layers 4, 6, and 10 of Jerominek as describing material layers. While Applicant does not agree that layers 4, 6, and 10 in Jerominek are material layers as recited in claim 1, the Office Action fails to point to any portion of Jerominek that describes layers 4, 6, and 10 as having "a plurality of vaporization temperatures," as required by the subject matter included in claim 1. For at least these reasons, the Office Action fails to show how Jerominek discloses all of the subject matter included in claim 1 as arranged in claim 1.

In another example of subject mater included in the claims and not disclosed by Jerominek, claim 6 recites,

> an electronic chip; and
>
> a conductive structure embedded in a plurality of materials, each of the plurality of materials having a different vaporization temperature, the plurality of materials is formed on the electronic chip and the conductive structure is coupled to the electronic chip;
>
> wherein each of the plurality of materials contacts a surface of the electronic chip.

Again, the Office Action, for example on page 3, relies on layers 4, 6, and 10 of Jerominek as disclosing a plurality of material layers. While Applicant does not agree that layers 4, 6, and 10 of Jerominek disclose the plurality of materials, "wherein each of the plurality of materials having a different vaporization temperature," as included in claim 6, claim 6 also requires that "each of the plurality of materials contacts a surface of the electronic chip." However and in contrast, Jerominek states,

> Each of the legs 11 further comprises a third layer 10 made of dielectric material. The third layer 10, in combination with the second layer 6, embeds the first layer 9, except for the lower and upper ends of the leg 11 where openings are provided in the

[2] *See* Jerominek at column 4, lines 58-63.

> dielectric layers 6 and 10 for allowing electrical connections between the first layer 9 and the electrical contacts 2 and 15.[3]

However, there is no description in Jerominek that indicates that layer 10 contacts a surface of the electronic chip, and thus the Office Action fails to show how Jerominek discloses "wherein *each* of the plurality of materials contacts a surface of the electronic chip," as required by the subject matter included in claim 6. (Emphasis added). For at least these reasons, the Office Action fails to show how Jerominek discloses all of the subject matter included in claim 6 as arranged in claim 6.

In a further example of subject matter included in the claims and not disclosed by Jerominek, claim 10 recites,

> an electronic chip; and
>
> a conductive structure embedded in a material layer having a structural component having a structural vaporization temperature and a fill material having a vaporization temperature less than the structural vaporization temperature, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip,
>
> wherein the conductive structure includes a horizontal conductive interconnect formed in and above the fill material and at least one vertical wiring via coupling the horizontal conductive interconnect to the electronic chip

For reasons analogous to those stated above with respect to claim 1, the Office Action fails to point out where in Jerominek there is a disclosure of "a material layer having a structural component having a structural vaporization temperature and a fill material having a vaporization temperature less than the structural vaporization temperature," as included in claim 10. In an attempt to supply this subject matter, the Office Action on page 3 with respect to Jerominek state, ". . . a material layer having a structural component 6 having structural vaporization temperature and a fill material 4 having a vaporization temperature less than the structural temperature." However, the Office Action fails to point to any portion of Jerominek that discusses the vaporization temperature of either layer 6 or of layer 4. For at least these reasons,

[3] *See* Jerominek at column 4, lines 1-7.

the Office Action fails to show how Jerominek discloses all of the subject matter included in claim 10 as arranged in claim 10.

Thus, the Office Action fails to show how Jerominek disclose all of the subject matter included in each of claims 1, 6, and 10, as arranged in each of claims 1, 6, and 10. Claim 94 depends from claim 1, and so includes all of the subject matter included in claim 1, and additional subject matter. Claims 8-9 depend from claim 6, and so include all of the subject matter included in claim 6, and additional subject matter. By way of example, but not limited to this example, claim 9 recites, "The integrated circuit assembly of claim 6, wherein at least one of the plurality of materials is carbon." The Office Action fails to point out where, and Applicant's representatives fail to find in Jerominek, a disclosure of "at least one of the plurality of material is carbon," as required by the subject matter included in claim 9.

Claims 12 and 14 depend from claim 10, and so include all of the subject matter included in claim 10. By way of example, but not limited to this example, claim 14 recites, "The integrated circuit assembly of claim 10, wherein the fill material is fabricated from carbon." The Office Action fails to point out where, and Applicant's representatives fail to find in Jerominek, a disclosure of "wherein the fill material is fabricated from carbon" as required by the subject matter included in claim 14.

For at least the reasons stated above with respect to claims 1, 6, and 10, and the additional examples as stated above, the Office Action fails to show how Jerominek discloses all of the subject mater include in each of claims 8-9, 12, 14, and 94, as arranged in each of these claims.

Because the Office Action fails to show how Jerominek discloses all of the subject matter included in each of claims 1, 6, 8-10, 12, 14, and 94 as arranged in each of these claims, the Office Action fails to establish a *prima facie* case of anticipation with respect to claims 1, 6, 8-10, 12, 14, and 94. Applicant respectfully requests withdrawal of the 35 U.S.C. § 102 rejection, and reconsideration and allowance of claims 1, 6, 8-10, 12, 14, and 94.

§103 Rejection of the Claims

Claims 2 and 3

Claims 2 and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jerominek (U.S. 5,962,909) as applied to claim 1, and further in combination with Irrinki (U.S. 5,784,328). Applicant respectfully traverses the rejection of claims 2 and 3.

For at least the reasons stated below, claims 2 and 3 are not obvious in view of the proposed combination of Jerominek and Irrinki, and the Office Action fails to establish a *prima facie* case of obviousness with respect to claims 2 and 3. In an attempt to establish a *prima facie* case of obviousness with respect to claims 2 and 3, the Office Action on page 5 states,

> Moreover, it would have been obvious to combine this disclosure of Irrinki with the disclosure of Jerominek because it would provide a dynamic random access memory chip with an on-chip temperature sensor, and thereby, as taught by Irrinki, solve prior art problems.

However, the Office Action fails to describe which "prior art problems" of Irrinki, if any, would be solved if combined with the disclosure of Jerominek. The Office Action admits on page 5 that "Jerominek does not appear to explicitly disclose wherein the electric chip is a memory chip; wherein the memory chip is a dynamic random access memory chip." Applicant agrees that Jerominek fails to disclose or suggest this subject matter as included in claim 2 and as included in claim 3. In addition, Applicant's representatives have performed an electronic search of Jerominek, and failed to find the word "memory" used in the written description of Jerominek. Thus, Jerominek fails to indicate any concern for the inclusion or use of a memory, or a dynamic random access memory, in the written description of Jerominek.

In contrast, Jerominek states, "In a preferred embodiment, the substrate layer 1 is a planar silicon wafer with a bolometer readout circuit (not shown) manufactured using conventional integrated circuit fabrication processing."[4] The Office Action fails to explain, or to provide any additional evidence, to show how a memory or a dynamic random access memory would be incorporated into the bolometer readout circuit of Jerominek with a reasonable degree of success.

[4] *See* Jerominek at column 3, lines 39-42.

Thus, the Office Action appear to be attempting to form the proposed combination of Jerominek and Irrinki using impermissible hindsight based on Applicants claimed subject matter.[5]

Even if the proposed combination of Jerominek and Irrinke could be made, (wherein Applicant does not agree that it could), the Office Action also fails to show how the proposed combination of Jerominek and Irrinki discloses or suggests all of the claimed subject matter included in claims 2 and 3.

Applicant believes they have established that Jerominek fails to disclose or suggest all of the subject matter included in claim 1, and so cannot disclose or suggest all of the subject matter included in claims 2 and 3, which depend from claim 1. The Office Action fails to point out, and Applicant's representatives fails to find in Irrinki, the subject matter included in claims 2 and 3 and missing from Jerominek. Thus, the proposed combination of Jerominek and Irrinki fails to disclose or suggest all of the claimed subject matter included in claims 2 and 3.

For at least the reasons stated above, the Office Action fails to establish a *prima facie* case of obviousness with respect to claims 2 and 3. Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claims 2 and 3.

Claim 4

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Jerominek as applied to claim 1, and further in combination with Nakai et al. (U.S. 4,663,535). Applicant respectfully traverses the rejection of claim 4.

For at least the reasons stated below, claim 4 is not obvious in view of the proposed combination of Jerominek and Nakai et al., and the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 4. Claim 4 includes, "wherein the conductive structure is fabricated from copper." The Office Action on page 6 admits that "Jerominek does not appear to explicitly disclose wherein the conductive structure is fabricated form copper." Instead, the Office Action on page 6 relies on Nakai et al. as providing this subject matter, and states,

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[5] The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

> Nakai discloses that aluminum, gold, titanium vanadium and copper are alternatives and equivalents; therefore, as reasoned from well established legal precedent, it would have been obvious to substitute or combine the copper of Nakai for or with he aluminum, gold, titanium or vanadium of Jerominek.

Applicant disagrees with theses statements for at least the reasons provided by the written description in Nakai et al. and Jerominek themselves. For example, Nakai et al. does not disclose aluminum, gold, titanium, vanadium, and copper as "alternatives and equivalents" as suggested in the Office Action. The cited portion of Nakai et al. referred to in the Office Action actually states,

> Material for pixel electrodes 14 may be selected from any one or more of a group composed of chromium (Cr), tantalum (Ta), tungsten (W), titanium (Ti), aluminum (Al), vanadium (V), nickel (Ni), copper (Cu), platinum (Pt), gold (Au).[6]

However, a statement that one or more elements may be used for "pixel electrodes" in Nakai et al. is not a disclosure that these elements are alternatives for any use as "electrically conductive material" as suggested in the Office Action. Further, there is no indication in the cited portion of Nakai et al. as quoted above that these elements are "equivalents" as also suggested in the Office Action. Further, Nakai et al. lists elements that may be used for pixel electrodes. However, Jerominek is concerned with microbridge structures[7], not pixel electrodes. The Office Action fails to provide any evidence, in either Jerominek or in Nakai et al., or from any other source, that shows how *copper* could be successfully used for the microbridge structure of Jerominek.

In fact, Jerominek explicitly teaches away from the idea that various metals are "alternatives and equivalents" as suggested in the Office Action, wherein Jerominek states,

> In these all metal or metal alloy supports, the selected metal or metal alloy must exhibit at the same time proper mechanical properties in order to mechanically support the platform, proper electrical properties in order to reduce the electrical resistance of the connection between the sensor layer placed on the platform and the readout electronic circuit mounted in the typically silicon substrate, and proper chemical properties so that said metal or

[6] *See* Nakai et al. at column 3, lines 18-22.
[7] *See e.g.* Jerominek, first sentence of the Abstract.

> metal alloy be compatible, i.e. not be damaged, with all the gaseous and liquid chemical products used during the microstructure fabrication process. **The combination of all of these properties severely limits the choice of suitable metals or metal alloys and manufacturing processes**. Moreover, all metal supports provide a poor thermal isolation of the microplatform due to a relatively high thermal conductivity of metals.[8]
> (Emphasis added).

Thus, Jerominek states that the combination of all of these properties severely limits the choice of suitable metal or metal alloys and manufacturing processes. Therefore, the statements made in the Office Action in support of forming the proposed combination of Jerominek and Nakai et al. are contradicted, and are taught away from, by at least the statements as quoted above from Jerominek and Nakai et al. Since the statements made in the Office Action in support of forming the proposed combination of Jerominek and Nakai et al. are not supported by, and are contradicted by, the written descriptions of Jerominek and Nakai et al., the Office Action fails to meet the requirements for forming the proposed combination of Jerominek and Nakai et al. Thus, the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 4.

Even if the proposed combination of Jerominek and Nakai et al. could be made, (wherein Applicant does not agree that it could), the Office Action also fails to show how the proposed combination of Jerominek and Nakai et al. discloses or suggests all of the claimed subject matter included in claim 4.

Applicant believes they have established that Jerominek fails to disclose or suggest all of the subject matter included in claim 1, and so cannot disclose or suggest all of the subject matter included in claim 4, which depends from claim 1. The Office Action fails to point out, and Applicant's representatives fails to find in Nakai et al., the subject matter included in claim 4 and missing from Jerominek. Thus, the proposed combination of Jerominek and Nakai et al. fails to disclose or suggest all of the claimed subject matter included in claim 4.

For at least the reasons stated above, the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 4. Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claim 4.

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[8] *See* Jerominek at column 1, lines 27-41.

Claim 94

Claim 94 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Jerominek as applied to claim 94 supra, and further in combination with Wu et al. (U.S. 5,191,404). Applicant respectfully traverses the rejection of claim 94.

For at least the reasons stated below, claim 94 is not obvious in view of the proposed combination of Jerominek and Wu et al., and the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 94. In an attempt to establish a *prima facie* case of obviousness with respect to claim 94, the Office Action on page 8 states,

> Moreover, it would have been obvious to combine this disclosure of Wu with the disclosure of Jerominek because it would enable external electrical connection of the chip of Jerominek.

However, the Office Action fails to point out any portion of Jerominek where external connections are mentioned, suggested, or required in Jerominek. In addition, Wu et al. states,

> As previously mentioned, bare chip 24 is assembled to multilayer interconnect member 22 using a technique called flip-chip bonding, a preferred implementation of which is solder bump. Flip-chip bonding involves positioning the bare chip 24 face-down onto the side 26 of interconnect member 22, aligning the bonding pads 23 of chip 24 to the conductive portions 25 of member 22, and thereafter bonding the pads 23 in conductive relation to the conductive portions 25. Unlike conventional printed wiring boards, multilayer interconnect member 22 is designed to accommodate the tight spacing or "pitch" between the bonding pads 23 of chip 24. The pitch between bonding pads 23 typically measures between 0.006-0.008 inches, compared to the pitch between TSOP, VSOP, and TAB package leads, which measures approximately 0.020 inches and which can be accommodated by conventional printed wiring board technology.[9]

Thus, Wu et al. concerns an assembly of a bare chip to a multilayer interconnect member using flip-chip bonding, preferably implementing solder bumps. In contrast, Jerominek is concerned with "a substrate layer provided with two first electrical contacts, a microstructure provided with two second electrical contacts, and a micro support for suspending the

[9] See Wu et al. at column 7, lines 34-51.

microstructure over and at a predetermined distance from the substrate layer."[10] The Office Action fails to describe how the bare chip and multilayer interconnect assembly of Wu et al. would be employed, or even could successfully be employed, in the microbridge structure of concern in Jerominek. Without such a showing, the Office Action fails to explain how there would be a reasonable expectation of success in forming the proposed combination of Jerominek and Wu et al., as suggested in the Office Action. Thus, the Office Action fails to meet the requirements for forming a *prima facie* case of obviousness with respect to claim 94.[11]

Even if the proposed combination of Jerominek and Wu et al. could be made, (wherein Applicant does not agree that it could), the Office Action also fails to show how the proposed combination of Jerominek and Wu et al. discloses or suggests all of the claimed subject matter included in claim 94.

Applicant believes they have established that Jerominek fails to disclose or suggest all of the subject matter included in claim 1, and so cannot disclose or suggest all of the subject matter included in claim 94, which depends from claim 1. The Office Action fails to point out, and Applicant's representatives fails to find in Wu et al., the subject matter included in claim 94 and missing from Jerominek. Thus, the proposed combination of Jerominek and Wu et al. fails to disclose or suggest all of the claimed subject matter included in claim 94.

For at least the reasons stated above, the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 94. Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claim 94.

Allowable Subject Matter

Claim 5 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 has been rewritten in independent form including all of the claimed subject matter from the base claim and any intervening claim from which claim 5 previously depended.

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[10] *See e.g.* Jerominek, first sentence of the Abstract.

[11] The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143.

Therefore, Applicant respectfully requests an indication in the next official communication in this application that claim 5 is allowed.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 11 Oct '06

By
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 11 day of October 2006.

KATE GANNON

Name

Signature